CPU Design Project – Part 6 Report

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In this project, we built a multi-cycle datapath cpu step by step through the whole semester. At first, we listed the instructions we need to execute and designed the structure of the multi-cycle datapath, which helped us learn more details about this kind of datapath. Then we used VHDL to write the code for each component of the datapath, this enriched our knowledge of VHDL and enhanced our ability to code. The memory generation part and the hardware implementation part gave us a chance to get familiar to Quartus II software and the method to use Altera DE2 FPGA. This semester-long project built a bridge between the theoretical world and the practical world, it gave us a chance to know better about the way a cpu work.

If we have a chance to do this project again next time, I will add some extra hardware into the datapath. The clock cycles needed to run instructions like branch equal or branch not equal can be reduced by adding another ALU into the datapath. Also, we can try to design a pipeline datapath next time to get a more comprehensive understanding about the structure and the way it works as pipeline datapath.

According to our own experience, the state diagram may not be the same as what we learned in the class. Some instructions like lw may need more cycles to be completely executed if we use the same multi-cycle structure as it shown on the course slides. To do this project, go through the whole requirements of these six parts before you start to design is really important and can save you a lot of time when you doing the later parts. Also, it is highly recommended to start doing the project earlier especially the part 5 and part 6. Because debugging the top level of the cpu and implementing your design on the FPGA could take you a lot of time, and the more time you put onto your project, the better result you can get.